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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,031	01/08/2002	Timothy W. Budell	END920010074US1	4220

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/042,031	Applicant(s) BUDELL ET AL.	
	Examiner Jeremy C. Norris	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,7-12,14 and 17-20* is/are rejected.

7)☒ Claim(s) *3,5,6,13,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 7-12, 14, and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,479,138 (hereafter Kuroda).

Kuroda discloses, referring to figures 1A & 1B, an electrical structure, comprising: a dielectric substrate (14) having a metal signal line (S1) therein; and a first metal voltage plane (G2) laminated to a first surface of the dielectric substrate, wherein the first metal voltage plane includes an opening, wherein an image of a first portion of the metal signal line projects across the opening (Gop) in the first metal voltage plane, and wherein a first electrically conductive strip across the opening in the first metal voltage plane includes the image of the first portion [claims 1, 11, 20], wherein the first electrically conductive strip is integral with the first metal voltage plane [claims 2, 12], wherein the first electrically conductive strip is linear across the opening in the first metal voltage plane [claims 4, 14], wherein a signal current is flowing through the metal signal line, wherein a return current is flowing through the first electrically conductive strip, wherein the signal current is an alternating current, and wherein the return current includes a portion of the signal current (see col. 1, lines 45-55) [claims 7, 17], wherein the electrical structure comprises an electrical apparatus selected from the group

consisting of a chip carrier and a printed circuit board, and wherein the electrical apparatus includes the dielectric substrate and the metal voltage plane (see col. 2, lines 35-50) [claim 8], further comprising: a second metal voltage plane (G1) laminated to a second surface of the dielectric substrate, 3 wherein the second metal voltage plane includes an opening (Gop), wherein an image of a second portion of the metal signal line projects across the opening in the second metal voltage plane, and wherein a second electrically conductive strip across the opening in the second metal voltage plane includes the image of the second portion [claim 9, 18], wherein a signal current is flowing through the metal signal line, wherein a first return current is flowing through the first electrically conductive strip, wherein a second return current is flowing through the second electrically conductive strip, wherein the signal current is an alternating current, wherein the first return current includes a first portion of the signal current, and wherein the second return current includes a second portion of the signal current (see col. 1, lines 45-55) [claims 10, 19].

Allowable Subject Matter

Claims 3, 5, 6, 13, 15, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claims 3 and 13 state the limitation "wherein the first electrically conductive strip is not integral with the first metal voltage plane". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the

prior art. Claims 5 and 15 state the limitation "wherein the first electrically conductive strip is nonlinear across the opening in the first metal voltage plane". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. Claims 6 and 16 state the limitation "wherein the opening in the first metal voltage plane has a vent area of no less than about 0.1 square millimeters". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose printed circuit boards with voltage planes having openings:

US 5,519,176 Goodman et al.,

US 6,184,477 Tanahashi,

US 6,184,478 Imano et al..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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